REMARKS

In response to the final Office Action mailed November 20, 2008, Applicant respectfully requests reconsideration. Claims 1, 3-15 and 17-23 were previously pending in this application. By this amendment, no claims have been amended, canceled or added. As a result, claims 1, 3-15 and 17-23 are pending for examination with claims 1 and 14 being independent.

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 1, 3-5, 7, 10, 12-15, 17, 18 and 21 under 35 U.S.C. §103(a) as purportedly being unpatentable over Mahalingaiah (US Patent No. 5,960,467) in view of Gandhi (U.S. Patent No. 6,405,305) and in further view of Meier (US Patent No. 6,405,305). Applicant respectfully traverses this rejection.

A. The Office Action Does Not Establish a Prima Facie Case of Obviousness

The Office Action concedes that the proposed combination of Mahalingaiah and Gandhi "fails to disclose the result of the speculative registers once they become committed to an architectural state," and also concedes that the combination "further fails to disclose the number of speculative registers." However, the Office Action proposes further combining Meier to cure the stated deficiencies, which Applicant respectfully points out that it does not. Indeed, the Office Action itself states that Meier is not applied as teaching "the number of speculative registers." In particular, in the Response to Arguments section on page 12, the Office Action states that "Meier is not used to indicate the number of speculative registers available and Official Notice has been taken." No reference in the combination, then, is applied to meet this limitation.

Accordingly, the Office Action itself concedes that Meier does not cure at least one of the stated deficiencies for which it was applied. That is, the Office Action applies Meier to remedy the fact that the combination of Mahalingaiah and Gandhi fail "to disclose the number of speculative registers," but simultaneously states that Meier is not used to "indicate the number of speculative registers." Thus, even according to the Office Action's own accounting, the combination of Mahalingaiah, Gandhi and Meier does not disclose or suggest each of the limitations of the claims. Therefore, the Office Action fails to establish a *prima facie* case of obviousness, and the rejection should be withdrawn for this reason alone.

B. One of Ordinary Skill in the Art Would Not Have Been Motivated to Modify Mahalingaiah According to Meier in the Way Proposed in the Office Action

As discussed above, the Office Action concedes that the proposed combination of Mahalingaiah and Gandhi "fails to disclose the result of the speculative registers once they become committed to an architectural state," and also concedes that the combination "further fails to disclose the number of speculative registers." However, this characterization of the deficiencies in the proposed combination is incomplete. What the combination fails to disclose is the number of data addresses a speculative register file is configured to store *relative* to the number of stages in the instruction pipeline in the same processor. Meier is completely silent in this respect.

The Office Action states that Meier discloses the use of 72 speculative registers and takes Official Notice that many processors have less than 72 pipeline stages. Applicant respectfully points out that while Meier does indeed disclose 72 speculative registers, Meier discloses nothing about how many of those registers are used to store speculative data addresses. Indeed, only "16 of them store the 'current' speculative state" and of those 16, "eight registers are FPU stack registers and eight registers are micro-architectural registers that store state information" (col. 17, lines 4-9). The 72 speculative registers in Meier store the complete "speculative state" of the entire floating point unit (FPU) 36. Meier says absolutely nothing about how many of those registers store speculative data addresses (i.e., addresses indicating the location of data used by corresponding stages in the pipeline). Accordingly, nothing definite can even be said about the number of speculative registers holding speculative data addresses in Meier, much less about how that number relates to the number of stages in the pipeline. Indeed, that many processors may have less than 72 pipeline stages says nothing about the number of pipeline stages in Meier, and more importantly, says nothing about the number of speculative registers to store data addresses relative to the number of pipeline stages in Meier.

That is, regardless of how many speculative registers storing speculative data addresses Meier actually discloses, Meier is completely silent with respect to how many registers are provided to hold speculative data addresses *relative to the number of stages in the pipeline.* Indeed, the Office Action doesn't even allege that Meier does so. The fact is that none of the

references in the proposed combination mention anything about the relationship between the number of speculative registers holding data addresses and the number of stages in the pipeline, and therefore no combination of the references can meet each of the limitations in the claims. Indeed, the missing teaching in each of the references is precisely what distinguishes Applicant's claims. Increasing the number of data addresses that the speculative register file can hold to be more than the number of stages in the pipeline is entirely missing from the art of record. In fact, the Office Action has failed to point to any teaching that discusses the relative number of data addresses that can be held by a speculative register file with respect to the number of stages in an instruction pipeline at all!

The Office Action attempts to make up for this deficiency by asserting a number of unsupported speculations about what one of ordinary skill in the art would have been motivated to do. The Office Action asserts that "Mahalingaiah would have been motivated to increase [the number of speculative registers] because 4 registers, in many cases, does not provide enough speculative information to result in any meaningful results." First, it is the number of speculative data addresses that a speculative register file can hold that is required in the claims, not some general notion of "speculative information." Second, it is not clear what the alleged "many cases" is referring to. Whether 4 registers is sufficient depends on the architecture of the processor. In fact, Mahalingaiah mentions nothing about any particular number of speculative registers being insufficient. The only guidance Mahalingaiah provides with respect to the number of speculative registers is that in "one embodiment, the number of storage locations within register storage 80 is equal in number to the number of lines within reorder buffer 32" (column 18, line 67 – column 19, line 2). That is, at best, Mahalingaiah suggests that the number of speculative registers should match the number of lines within the reorder buffer. Nothing is mentioned with respect to how many speculative registers should be provided relative to the number of stages in the pipeline, nor does Mahlingaiah suggest any problems associated with having insufficient storage to "provide enough speculative information to result in any meaningful results."

One of ordinary skill in the art simply would not have been motivated to add additional speculative registers unnecessarily. The alleged motivation to increase the number of speculative registers in Mahalingaiah is to "provide enough speculative information to result in

meaningful results." However, it is nowhere reported in Mahalingaiah that the disclosed register storage does not already do so. That is, the alleged motivation attempts to solve a problem in Mahalingaiah that is not reported to even exist! As such, there is absolutely no plausible design reason for increasing the number speculative registers in Mahalingaiah beyond the number of lines within the reorder buffer, particularly not an arbitrary number of speculative registers plucked from an altogether separate reference (Meier) describing an entirely different system with entirely different design considerations and architecture.

The Office Action proposes to modify Mahalingaiah to have 72 speculative registers (which as discussed above is not what Meier discloses) and then to implement a pipeline with less than 72 pipeline stages. The Office Action has completely and arbitrarily re-designed the system of Mahalingaiah without providing any support as to why one of ordinary skill in the art would have wanted to do so. Indeed, the Office Action's proposed modification asserts that one of ordinary skill in the art would have been motivated to unnecessarily increase the number of speculative registers (and increase it to the 72 speculative registers allegedly taught by Meier, nonetheless), and then to select an instruction pipeline having less stages then the increased number of speculative registers added for no discernible reason (i.e., added with no evidence of benefit to the system of Mahalingaiah). Not only does the proposed modification not make sense, it is to some extent, backwards. A designer would not select the number of speculative registers and then separately, and for alleged reasons that are entirely different, select the number of pipeline stages. These design concerns are interrelated. Indeed, the number of speculative registers provided depends on the number of stages in the instruction pipeline of a particular design.

Conventionally, to support a particular pipeline using optimal speculative registers (i.e., without providing extra registers) the number of speculative registers matches the number of stages in the pipeline. Indeed, Applicant's specification reports that conventional design techniques propose providing a number of speculative registers equal to the number of stages in the instruction pipeline. Providing any amount of additional registers would simply increase the size and cost of the design. Applicant alone has appreciated that by going against the conventional wisdom, a power savings may be achieved. That is, by sacrificing optimal real estate, the design could save on power consumption. None of the cited references disclose or

suggest departing from the conventional of wisdom of matching the number of speculative registers with the number of stages in the pipeline. Indeed, none of the references even mention this relationship at all. Accordingly, not only would one skilled in the art not have been motivated to modify Mahalingaiah based on Meier as proposed in the Office Action, there is no combination of the cited references that teach every limitation in the claims.

C. Claims 1 and 3-13

Claim 1 recites, *inter alia*, "a pipelined execution unit configured to execute instructions in an instruction pipeline including each of a plural number of stages required to execute instructions from an initial stage in which instructions are fetched through a final stage in which execution of the instructions are completed, the plural number of stages using data at locations specified by the speculative data addresses." Having thus defined the instruction pipeline, the alleged combination of Mahalingaiah, Gandhi and Meier does not disclose or suggest a digital signal processor having "a speculative register file capable of simultaneously storing *at least a number of speculative data addresses equal to or greater than the plural number of pipeline stages and at least one architectural data address*, the speculative register file configured to hold the speculative data addresses as corresponding instructions advance through the instruction pipeline and at least one speculative data address after the at least one speculative data address becomes a respective architectural data address," as recited in claim 1 (emphasis added). Therefore, claim 1 patentably distinguishes over the alleged combination and is in allowable condition.

Claims 3-13 depend from claim 1 and are allowable based at least on their dependency.

D. Claims 14, 15 and 17-23

Claim 14 recites, *inter alia*, "executing an instruction using data at a location specified by the speculative data addresses in a pipelined execution unit including each of a plural number of pipeline stages required to execute the instruction from an initial stage in which the instruction is fetched through a final stage in which execution of the instruction is completed." Having thus defined the executing act, the alleged combination of Mahalingaiah, Gandhi and Meier nowhere discloses or suggests holding speculative data addresses in a speculative register file as a corresponding instruction advances through the pipeline, "the speculative register file capable of storing *a number of speculative data addresses equal to or greater than the plural number of*

pipeline stages in the pipelined execution unit and at least one architectural data address," as recited in claim 14 (emphasis added). Therefore, claim 14 patentably distinguishes over the combination and is in allowable condition. Claims 15 and 17-23 depend from claim 14 and are allowable based at least on their dependency.

In view of the foregoing, Applicant respectfully requests that the rejection under 35 U.S.C. §103 be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: February 20, 2009

Respectfully submitted,

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